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CR391 Fixes

Softcon Software Control Services (Pty) Ltd.

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Revision History

Name	Date	Reason For Changes	Version
BD	05/04/2012	Initial document	0.0
BD	12/04/12	Add MUX keys storage	00.1b
BD	12/04/12	Increased card badge performance	00.1c
BD	13/04/12	When sending Firmware reset the controller waits 5 sec before rest so that ACK can be sent to SW	00.1d
BD	13/04/12	Coms bits 9/8/7 is display 7 or 8 or 9 Issue 6 resolved(when edit setting the next char shows funny character)	00.1e
BD	13/04/12	IP address change now take immediate affect (issue 2)	00.1f
BD	16/04/12	When Doing a reset to the controller the TCPIP communication slows down. Now fixed	00.20
BD	17/04/12	Code clean-up	00.21
BD	09/05/12	Development (NO RELEASE)	00.22 – 00.27
BD	09/05/12	• Improved TCPIP stack performance • Add slave • Improved local input performance • Recalibrate inputs • Moved UART init process • Some Code clean-up • On HW 1.4.6 Zener 3 must be removed or replace with min 4.8VZ nominal.	00.28
BD	07/06/2012	• Repeat TCPIP Message fixed • Iteration of multi message process fixed • Input message size limit set to 7	00.2E
BD	11/06/2012	• When No readers present then Inputs should work	00.2F
BD	13/06/2012	• When rest/setup LED2 on board will indicate when done	00.30
BD	14/06/2012	• Capture invert now working	00.31
BD	05/07/2012	• MagStipe added	00.32
BD	06/07/2012	• Fixed delay timing	00.33

		• Some code clean-up	
BD	06/07/2012	• Increase MUXkeys from 32 to 64	00.34
BD	10/07/2012	• Enabled 8 bit e/o/ no parity • Added Interrupts to all UARTs	00.35
BD	10/07/2012	• Enabled WDT on Bootloader • Enabled WDT Passover to Application	• Ver2.0 • 00.36
BD	27/08/2012	• Bigger Card DB • 65K offline transaction buffer on mast ctrl • Default Factory setting correction • Unknown TCPIP messages is ACK • LED 3 for LAN comms • Fixed inputs to work on start-up • Only ACK on own node number if slave • Controller Type 7 added • Irrattic reader power off fixed	00.51
BD	29/08/2012	• Date and time did not always show correct on tcpip frame (fixed) • Reset interrupt counter if wrong number of bits for reader •	00.54
BD	12/09/2012	• Temp fix for buffer overrun for messages stored on stack for coms up	00.58
BD	10/10/2012	• New bootloader 3.5 • Bootloader run via RS485 added • Fixed possible miss read of bit on wiegand if from FP reader • Flash RUN led even with slaves running	00.62
BD	11/10/2012	• Decreased Bootloader timer out • Fixed loop lock when writing comms down • Increased slave offline buffer to 0xffff transactions	• Ver3.6 • 00.64
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BD	08/11/2012	• Fixed double messages when Master brings slaves online • Increase LAN time out by 100ms	• 00.66
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BD	21/11/2012	• When TCPIP link is bad and have many slaves below master the TCPIP buffer could overrun. And cause a reset. Fixed	• 00.67
BD	26/11/2012	• Timming in mianloop changed	• 00.68

BD	28/11/2012	• Timming in slave loop changed	• 00.69 •
	29/11/2012	• Adjusted TCPIP timing to accommodate WAN • Adjust TCPIP stack to run on 10M Half duplex fixed port	• 00.6B
BD	17/01/2013	• Changed Boot loader IP address 192.168.100.1	• BL 3.7
BD	17/01/2013	• Changed Default IP address to 192.168.100.1 • Add to check for factory default when in run mode so that no need for power cycle • Enabled weak- pulls on U3 port B to prevent accidental factory rest	• 00.6D
BD	17/01/2013	• BL request from SW3/mKNock will wait till buffer empty before going to BL Mode	• 00.6E
BD	23/01/2013	• Improved TCPIP performance over APN (BAD link) prevent reset • When offline for a short period do not lose messages between offline stack and online stack	• 00.71
BD	31/01/2013	• Sense if PHY is onboard (Firmware) • Sense if PHY is onboard (Boot loader)	• 00.76 • 3.8
BD	12/02/2013	• SPI interface between PHY and CPU out of sync on very busy network. Adapt driver	• 00.77
BD	18/02/2013	• Fixed Dual FP operation • Reduced WDT timeout • Prevent TCPIP ACK when in slave mode	• 00.79
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